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DICKSTEIN SHAPIRO LLP
1825 EYE STREET, NW
WASHINGTON, DC 20006

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/685,792	**Applicant(s)** BEREZIN ET AL.	
	Examiner Timothy J. Henn	**Art Unit** 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2007*.
2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-53* is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-10 and 12-53* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☐ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments with respect to claims 12-53 have been fully considered but they are not persuasive.

3. Applicant argues that since Dierickx does not disclose a transfer transistor configured in the manner of Pain or Kochi (i.e. between the photodiode and an output), Dierickx is not compatible with the pixels of Pain or Kochi. While Dierickx shows the use of a 3T pixel (e.g. Figure 1), Dierickx further discloses that the "method of the invention can also be applied to any pixel that has a node with a reset transistor and a memory element such as a capacitor for charge storage". Dierickx further discloses that the capacitor for charge storage may be the parasitic capacitance of the photodiode. The examiner notes that both Pain and Kochi disclose pixels which meet these criteria (e.g. Figure 2A of Pain and Figure 1 of Kochi), therefore it is not believed that one of ordinary skill in the art would find reason to think that the method of Dierickx would be incompatible with the Pain and Kochi references as argued. Therefore, Applicant's arguments are not considered persuasive.

4. Applicant further argues that the transistor 37 and the area between transistors 37 and 31 of Dierickx (see Figure 3) can not be considered a transfer transistor and floating diffusion respectively. Specifically with respect to transistor 37 Applicant argues that the transistor does not selectively couple the photodiode 32 to the source follower

transistor 34. While this undoubtedly true, this limitation is not found in the claims. Since transistor 37 transfers charge, it is broadly considered a "transfer transistor" as claimed. With respect to the floating diffusion region, Applicant argues that this region is "merely a conductive wire", however no basis has been given for this argument. Further, Dierickx discloses the use of CMOS technology to implement the image sensor wherein the image sensor is formed as a single array (e.g. c. 1; Figure 10). In such an array, it is unclear why one of ordinary skill in the would believe that a "conductive wire" would be used to connect transistors 31 and 37.

5. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 12-14, 16-18 and 31-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Dierickx (US 7,106,373).

[claim 12]

Regarding claim 12, Dierickx discloses a method for operating a pixel circuit, the method comprising: accumulating photo-generated charge in a photodiode during a charge integration period (Figure 11, "signal on node"); applying a first saturation control signal at a first voltage level to a transfer transistor during the integration period to remove some accumulated charge from the photodiode to a storage node (Figure 11, "reset"; c. 6, ll. 51-61); applying a second saturation control signal to the transfer transistor during the integration period to remove additional accumulated charges from the photodiode (Figure 11, "reset"; c. 6, ll. 51-61) and applying a reset pulse to a reset transistor coupled to the storage node each time a first and second saturation control signal is applied (Figure 5; c. 6, ll. 51-61).

[claim 13]

Regarding claim 13, Dierickx discloses a second saturation control signal which has a smaller voltage than the first saturation control signal (Figure 11, "reset").

[claim 14]

Regarding claim 14, Dierickx discloses saturation control signals and reset signals which are applied concurrently (Figure 5; c. 6, ll. 51-61).

[claim 16]

Regarding claim 16, Dierickx discloses applying a third saturation control signal to the transfer transistor at the end of the integration period to transfer accumulated charges at the photodiode to a storage node (Figure 11, "reset").

[claim 17]

Regarding claim 17, Dierickx discloses first, second and third saturation control signals which define a segment of the integration period (Figure 11, “reset”).

[claim 18]

Regarding claim 18, the gain of the integration segments defined by Dierickx is inherently different given their different integration time periods and voltage levels of the respective saturation control signals.

[claim 31]

Regarding claim 31, Dierickx discloses a pixel circuit comprising: a photocharge collecting region (Figure 3, Item 32); a floating diffusion region coupled to a reset node through a reset transistor (Figure 3) and a transfer transistor, coupled between the photocharge collecting region and the floating diffusion region (Figure 3), wherein a signal controller is configured to apply a first saturation control signal at a first voltage level to the transfer transistor to start an integration period, to sequentially apply additional saturation control signals to the transfer transistor, each of the additional saturation control signals having voltage levels that are successively smaller than a prior saturation control signal and to apply a reset pulse to a reset transistor each time additional saturation control signals are applied, wherein the signal controller is configured to apply the saturation control signals and the reset signals simultaneously (Figures 5 and 11; c. 6, l. 51 - c. 7, l. 17).

[claim 32]

Regarding claim 32, Dierickx discloses application of additional saturation control signals which defines an integration portion in the integration period (Figures 5 and 11).

[claim 33]

Regarding claim 33, Dierickx discloses a second saturation control signal at a voltage level lower than the first voltage level and defining a second integration portion (Figures 5 and 11; c. 6, l. 51 - c. 7, l. 17).

[claim 34]

Regarding claim 34, Dierickx discloses a third saturation control signal at a voltage level lower than the second voltage level and defining a third integration portion (Figures 5 and 11; c. 6, l. 51 - c. 7, l. 17).

[claim 35]

Regarding claim 35, Dierickx discloses a final saturation control signal at the first voltage level after application of the third saturation control signal, the final saturation control signal ending the integration period (Figures 5 and 11; c. 6, l. 51 - c. 7, l. 17).

[claim 36]

Regarding claim 36, the gain of the integration segments defined by Dierickx is inherently different given their different integration time periods and voltage levels of the respective saturation control signals.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dierickx (US 7,106,373) in view of Raynor et al. (US 2002/0114025).

[claim 1]

Regarding claim 1, Dierickx discloses a method of operating a pixel circuit, the method comprising: accumulating photo-generated charge during an integration period (Figure 5, "signal on node"); removing some of the accumulated photo-generated charges during the integration period (Figure 5, "signal on node" and "reset") and producing an output signal based on accumulated charges existing at the end of the integration period (Figure 5, "signal on node" and "readout moment"). However, Dierickx discloses the use of a 3T pixel which does not include a transfer transistor as claimed.

Raynor discloses that 4T pixel designs can be used instead of 3T designs to achieve higher sensitivity and the ability to perform electronic shuttering (Paragraphs 0002-0007). The 4T pixel design described by Raynor (Figure 4) includes a transfer transistor (Figure 4, Item M4) and a reset transistor (Figure 4, Item M2) connected to a photodiode (Figure 4) wherein the transfer transistor selectively couples the photodiode to a source follower transistor (Figure 4, Item M1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the

4T pixel design in place of Dierickx's 3T pixel design to achieve higher sensitivity and allow for electronic shuttering.

Dierickx discloses an operation in which a voltage is applied to a transistor between the reset transistor and the photodiode (Figure 5, "reference"; c. 6, l. 51 - c. 7, l. 2). Raynor discloses that it is desirable to minimize the area of the pixel circuitry (Paragraph 0009). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the reference voltage of Dierickx to the transfer transistor M4 of the Raynor pixel since transistor M4 is positioned between the reset transistor and the photodiode (Raynor; Figure 4) and since adding an extra transistor would needlessly increase the size of the pixel.

[claim 2]

Regarding claim 2, Dierickx discloses a method wherein the integration period includes a plurality of charge removal points (Figure 11, "reset"; c. 7, ll. 15-17).

[claim 3]

Regarding claim 3, Dierickx discloses a method wherein the plurality of charge removal points each has an associated signal which controls the amount of accumulated photo-generated charges removed (Figure 11, "reset").

[claim 4]

Regarding claim 4, Dierickx discloses a method wherein each of the associated signals has a different signal characteristic from another associated signal such that different amounts of charges are removed by each of the associated signals (Figure 11, "reset").

[claim 5]

Regarding claim 5, Dierickx discloses a method wherein the signal characteristic is a signal pulse amplitude (Figure 11, "reset").

[claim 8]

Regarding claim 8, Dierickx discloses a method wherein the photo-generated charges are accumulated by a photodiode (Figure 3, Item 32) and the act of removing comprises turning on a transfer transistor to remove photo-generated charge from the photodiode to a floating diffusion node and turning on a reset transistor to remove photo-generated charge from the floating diffusion node (Figures 3 and 5; c. 6, ll. 51-64).

[claim 9]

Regarding claim 9, Dierickx discloses a method wherein the reset transistor and the transfer transistor are turned on at the same time (Figures 3 and 5; c. 6, ll. 51-64).

[claim 10]

Regarding claim 10, Dierickx in view of Raynor discloses a method wherein the reset transistor is turned on after the transfer transistor is turned on to remove charge from the photodiode to the floating diffusion node (Dierickx, Figures 3 and 5; c. 6, ll. 51-64; Raynor, Figure 4).

10. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dierickx (US 7,106,373) in view of Raynor et al. (US 2002/0114025) in view of Ueno

(US 6,342,920).

[claim 6]

Regarding claim 6, Dierickx does not disclose a signal characteristic which is a pulse width. Ueno discloses a similar method in which a portion of a charge amount is removed by using transfer signals and further discloses that the signals can have different pulse widths (c. 4, ll. 29-49; Claims 9 and 10). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary a pulse width of the signals of Dierickx as an alternate art recognized method for controlling the amount of charge to be removed.

[claim 7]

Regarding claim 7, Dierickx does not disclose a signal characteristic which is a pulse width and pulse amplitude. Ueno discloses a similar method in which a portion of a charge amount is removed by using transfer signals and further discloses that the signals can have different pulse widths (c. 4, ll. 29-49; Claims 9 and 10). Ueno further discloses that varying the pulse amplitude can control the amount of charge removed (c. 4, ll. 29-49). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary a pulse width and amplitude of the signals of Dierickx as an alternate art recognized method for controlling the amount of charge to be removed.

11. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dierickx (US 7,106,373).

[claim 15]

Regarding claim 15, Dierickx does not disclose applying the saturation control signals before the reset signals. Official Notice is taken that it is well known in the art to apply transfer signals before reset signals when removing charge from a photodiode to a reset node through a transfer transistor and a reset transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the saturation control signals of Dierickx before the reset signals to first store the signals on the floating diffusion node prior to transferring them to the reset node.

12. Claims 19-23 and 37-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. (US 7,002,626) in view of Dierickx (US 7,106,373).

[claim 19]

Regarding claim 19, Pain discloses a pixel circuit (Figure 2A) including a transfer transistor (Figure 2A, Item 56) and an anti-blooming transistor (Figure 2A, Item 62). Pain further discloses accumulating photo-generated charge in the photodiode and applying a voltage at the transfer transistor (e.g. Figures 3A-3D). However, Pain does not disclose applying saturation control signals as claimed.

Dierickx discloses a method wherein a photo-generated charge is accumulated in a photodiode during a charge integration period (Figure 11, "signal on node"), a first saturation control signal at a first voltage is applied to a transistor to remove some accumulated charge from the photodiode and applying a second saturation control signal to the anti-blooming transistor to remove additional accumulated charges from the photodiode (Figure 11, “reset” and “signal on node”). Dierickx discloses that such a method obtains a large dynamic range (c. 1, ll. 13-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the method of Dierickx to the pixel circuit of Pain to obtain images with a large dynamic range. Dierickx discloses removing accumulated signal charges by applying varying voltage pulses to a transistor connected directly to the photodiode (e.g. Figure 1), Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the varying voltage pulses of Dierickx to the anti-blooming transistor of Pain to remove accumulated signal charges since the anti-blooming transistor is configured in the same way as described in the method of Dierickx.

[claim 20]

Regarding claim 20, Dierickx discloses a second saturation control signal that has a voltage smaller than the voltage of the first saturation control signal (Figure 11, “reset”).

[claim 21]

Regarding claim 21, Dierickx discloses reading out the accumulated charges at the end of the integration period (Figure 11, “readout moment”). Pain discloses reading out signal charges from the photodiode by activating a transfer transistor (Figure 2A, Item 56), Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a third control signal to the transfer transistor as claimed.

[claim 22]

Regarding claim 22, Dierickx discloses first, second and third signals which defines segments of the integration period (Figure 11).

[claim 23]

Regarding claim 23, the gain of the integration segments defined by Dierickx is inherently different given their different integration time periods and voltage levels of the respective saturation control signals.

[claim 37]

Regarding claim 37, Pain discloses a pixel circuit comprising: a photocharge collecting region (Figure 2A, Item PG), a floating diffusion region (Figure 2A, Item 54) being coupled through a reset transistor (Figure 2A, Item RST) and further being coupled to the photocharge collection region through a transfer transistor (Figure 2A, Item TX) and an anti-blooming region for receiving charge from the photodiode collection region (Figure 2A, Item 64) and an anti-blooming transistor (Figure 2A, Item TX2). However, Pain does not disclose applying saturation control signals as claimed.

Dierickx discloses a system wherein a photo-generated charge is accumulated in a photodiode during a charge integration period (Figure 11, "signal on node") and saturation control signals at a first voltage to start a first integration period and successively smaller voltages are applied during the integration period (Figure 11, "reset" and "signal on node"). Dierickx discloses that such a system obtains a large dynamic range (c. 1, ll. 13-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the system of Dierickx to the pixel circuit of Pain to obtain images with a large dynamic range. Dierickx discloses removing accumulated signal charges by applying varying voltage pulses to a transistor connected directly to the photodiode (e.g. Figure 1), Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the varying voltage pulses of Dierickx to the anti-blooming transistor of Pain to remove accumulated signal charges since the anti-blooming transistor is configured in the same way as described in the method of Dierickx.

[claim 38]

Regarding claim 38, Dierickx discloses application of additional saturation control signals which defines an integration portion in the integration period (Figure 11).

[claim 39]

Regarding claim 39, Dierickx discloses a second saturation control signal at a voltage level lower than the first voltage level and defining a second integration portion (Figure 11; c. 6, l. 51 - c. 7, l. 17).

[claim 40]

Regarding claim 40, Dierickx discloses a third saturation control signal at a voltage level lower than the second voltage level and defining a third integration portion (Figure 11; c. 6, l. 51 - c. 7, l. 17).

[claim 41]

Regarding claim 41, Dierickx discloses a final saturation control signal at the first voltage level after application of the third saturation control signal, the final saturation control signal ending the integration period (Figure 11; c. 6, l. 51 - c. 7, l. 17).

[claim 42]

Regarding claim 42, the gain of the integration segments defined by Dierickx is inherently different given their different integration time periods and voltage levels of the respective saturation control signals.

13. Claims 24-30 and 43-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kochi (US 9,947,088) in view of Dierickx (US 7,106,373).

[claim 24]

Regarding claim 24, Kochi discloses a pixel circuit including a first photodiode (Figure 1, Item 1-1), a second photodiode (Figure 1, Item 1-2), a first transfer transistor coupled to the first photodiode (Figure 1, Item 5-1) and a second transfer transistor coupled to the second photodiode (Figure 1, Item 5-2). Kochi further discloses first and second charge integration periods for the first and second photodiodes as is evidenced by the TX1 and TX2 control signals in Figure 3. However, Kochi does not disclose applying saturation control signals as claimed.

Dierickx discloses a method wherein a photo-generated charge is accumulated in a photodiode during a charge integration period (Figure 11, "signal on node"), a first (or second) saturation control signal at a first voltage is applied to a transistor to remove some accumulated charge from the photodiode and applying a third (or fourth) saturation control signal to the anti-blooming transistor to remove additional accumulated charges from the photodiode (Figure 11, "reset" and "signal on node") and applying a reset pulse to a reset transistor coupled to the storage node each time the saturation control signal is applied (Figure 5, c. 6, ll. 51-61). Dierickx discloses that such a method obtains a large dynamic range (c. 1, ll. 13-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the method of Dierickx to the pixel circuit of Kochi to obtain images with a large dynamic range. Dierickx discloses that the saturation control signals can be applied to a transistor between the reset transistor and the photodiode (c. 6, ll. 51-61), Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the saturation control signals of Dierickx to the transfer transistors of Kochi since the transfer transistors are between the photodiode and the reset transistor. It would further be obvious to use first, second third and fourth control signals applied to the first and second transfer transistors as claimed to increase the dynamic range for photodiode 1-1 and 1-2 of Kochi.

[claim 25]

Regarding claim 25, Dierickx discloses using multiple saturation control signals which decrease in voltage (Figure 11, "reset"), Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the third saturation control signal a lower voltage than the first saturation control signal and the fourth saturation control signal a lower voltage than the second saturation control signal as claimed.

[claim 26]

Regarding claim 26, Dierickx discloses saturation control signals and reset signals which are applied concurrently (Figure 5; c. 6, ll. 51-61).

[claim 27]

Regarding claim 27, Dierickx does not disclose applying the saturation control signals before the reset signals. Official Notice is taken that it is well known in the art to apply transfer signals before reset signals when removing charge from a photodiode to a reset node through a transfer transistor and a reset transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the saturation control signals of Dierickx before the reset signals to first store the signals on the floating diffusion node prior to transferring them to the reset node.

[claim 28]

Regarding claim 28, Dierickx discloses reading out the accumulated charges at the end of the integration period (Figure 11, "readout moment"). Kochi discloses reading out signal charges from the photodiode by activating a transfer transistor (Figures 1 and 3), Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a fifth and sixth control signals to the transfer transistor as claimed to readout signals from photodiodes 1-1 and 1-2.

[claim 29]

Regarding claim 29, Kochi and Dierickx discloses saturation control signals which define segments of integration periods for photodiode 1-1 (i.e. a first integration period) and photodiode 1-2 (i.e. a second integration period; Kochi, Figure 3; Dierickx, Figure 11).

[claim 30]

Regarding claim 30, the gain of the integration segments defined by Kochi and Dierickx are inherently different given their different integration time periods and voltage levels of the respective saturation control signals.

[claim 43]

Regarding claim 43, Kochi discloses a pixel circuit comprising: a first (Figure 1, Item 1-1) and second (Figure 1, Item 1-2) photocharge collection region; a first floating diffusion region (Figure 1), coupled to a reset node through a reset transistor (Figure 1, Item 4); a second floating diffusion region coupled to the first floating diffusion region (Figure 1); a first transfer transistor (Figure 1, Item 5-1), coupled between the first photocharge collection region and the first floating diffusion region and a second transfer transistor (Figure 1, Item 5-2), coupled between the second photocharge collection region and the second floating diffusion region. Kochi further discloses first and second charge integration periods for the first and second photodiodes as is evidenced by the TX1 and TX2 control signals in Figure 3. However, Kochi does not disclose applying saturation control signals as claimed.

Dierickx discloses a system wherein a photo-generated charge is accumulated in a photodiode during a charge integration period (Figure 11, "signal on node"), a first (or second) saturation control signal at a first voltage is applied to a transistor to start an integration period and remove some accumulated charge from the photodiode and applying additional saturation control signals at a lower voltage to the anti-blooming transistor to start additional integration periods and remove additional accumulated charges from the photodiode (Figure 11, "reset" and "signal on node") and applying a reset pulse to a reset transistor coupled to the storage node each time the saturation control signal is applied (Figure 5, c. 6, ll. 51-61). Dierickx discloses that such a system obtains a large dynamic range (c. 1, ll. 13-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the method of Dierickx to the pixel circuit of Kochi to obtain images with a large dynamic range. Dierickx discloses that the saturation control signals can be applied to a transistor between the reset transistor and the photodiode (c. 6, ll. 51-61), Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the saturation control signals of Dierickx to the transfer transistors of Kochi since the transfer transistors are between the photodiode and the reset transistor. It would further be obvious to use saturation control signals applied to the first and second transfer transistors as claimed to increase the dynamic range for photodiode 1-1 and 1-2 of Kochi.

[claims 44 and 49]

Regarding claims 44 and 49, Dierickx discloses application of additional saturation control signals which defines an integration portion in the integration period (Figure 11).

[claim 45 and 50]

Regarding claim 45 and 50, Dierickx discloses a second saturation control signal at a voltage level lower than the first voltage level and defining a second integration portion (Figure 11; c. 6, l. 51 - c. 7, l. 17).

[claim 46 and 51]

Regarding claim 46 and 51, Dierickx discloses a third saturation control signal at a voltage level lower than the second voltage level and defining a third integration portion (Figure 11; c. 6, l. 51 - c. 7, l. 17).

[claim 47 and 52]

Regarding claim 47 and 52, Dierickx discloses a final saturation control signal at the first voltage level after application of the third saturation control signal, the final saturation control signal ending the integration period (Figure 11; c. 6, l. 51 - c. 7, l. 17).

[claim 48 and 53]

Regarding claim 48 and 53, the gain of the integration segments defined by Dierickx is inherently different given their different integration time periods and voltage levels of the respective saturation control signals.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Henn whose telephone number is (571) 272-7310. The examiner can normally be reached on M-F 11-7.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LIN YE
SPE. ART UNIT 2622